microsecond. 2^n-1 comparators are required to provide a digital output of n bits. In many on-line systems, it is the practice to choose a word length so that the quantization errors (one-half the least significant bit) are of the same order of magnitude as those introduced by analog-component tolerances. For this reason, word-lengths as large as twelve to fourteen-bits are sometimes employed. To produce a fourteen-bit digital output by the simultaneous conversion technique would require over 16,000 comparators. It is clear, therefore, that the simultaneous-conversion approach is economically impractical where more than a few bits are required. The conversion methods described in the succeeding sections obviate this difficulty by using one or a limited number of converters repeatedly in each conversion, sacrificing conversion-speeed for greatly reduced cost.

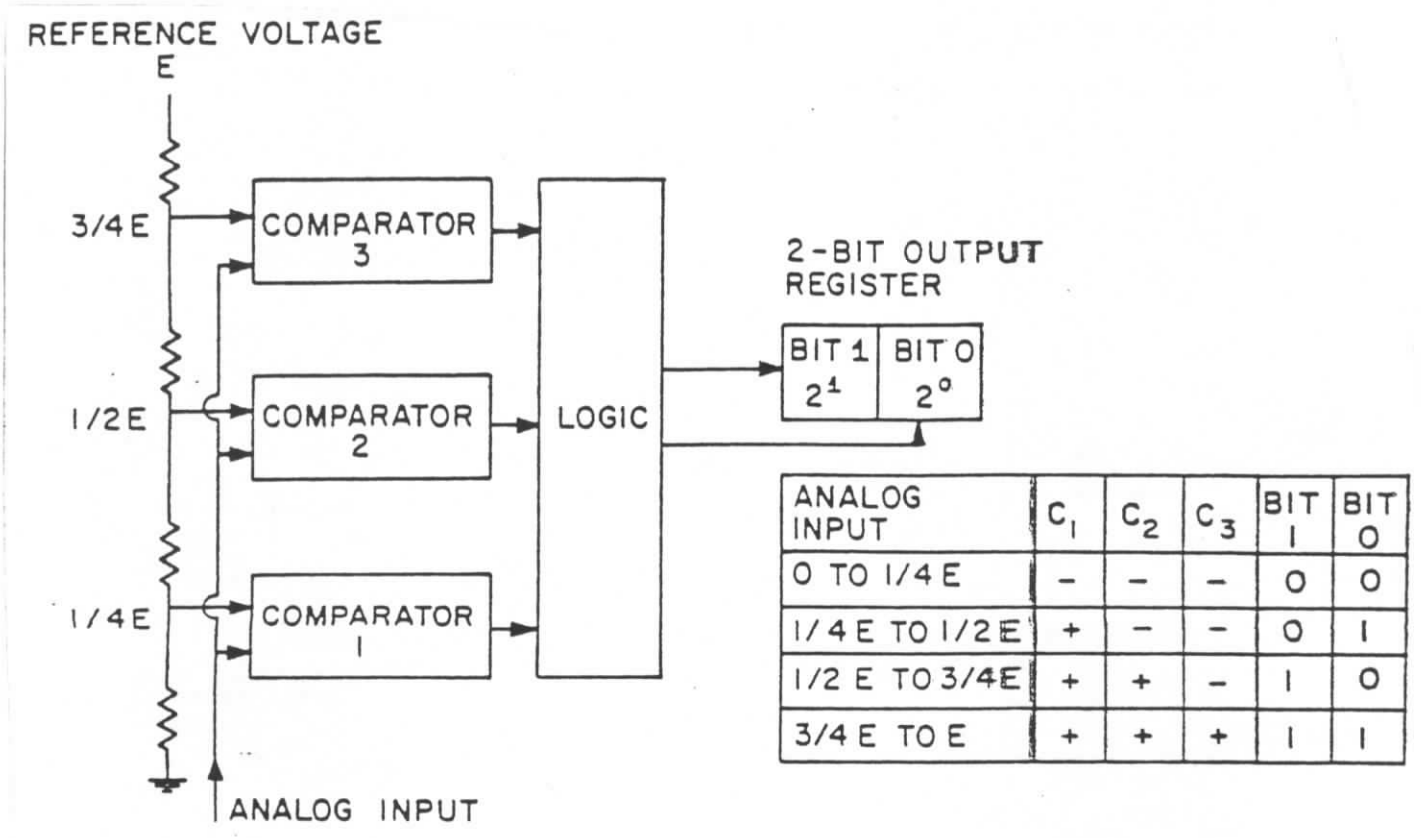

Figure 5.8 Simultaneous-type Analog/Digital Converter

5.7 Closed-Loop Analog/Digital Converters

The design of the most widely-used analog/digital converter is based upon the recognition that digital/analog conversion is a much more simple process than is analog/digital conversion. Accordingly, a digital/analog converter is connected into a closed loop as shown in Figure 5.9. The digital output of the converter is stored in a digital register, and the digital number contained in the register serves also as the input for the digital/analog converter. This converter then produces an analog output-voltage proportional to the number contained in the digital register. This analog voltage constitutes one input of a comparator; the other input of the comparator is the analog voltage to be converted. The comparator output is therefore an error signal, determined by the difference between the two inputs.

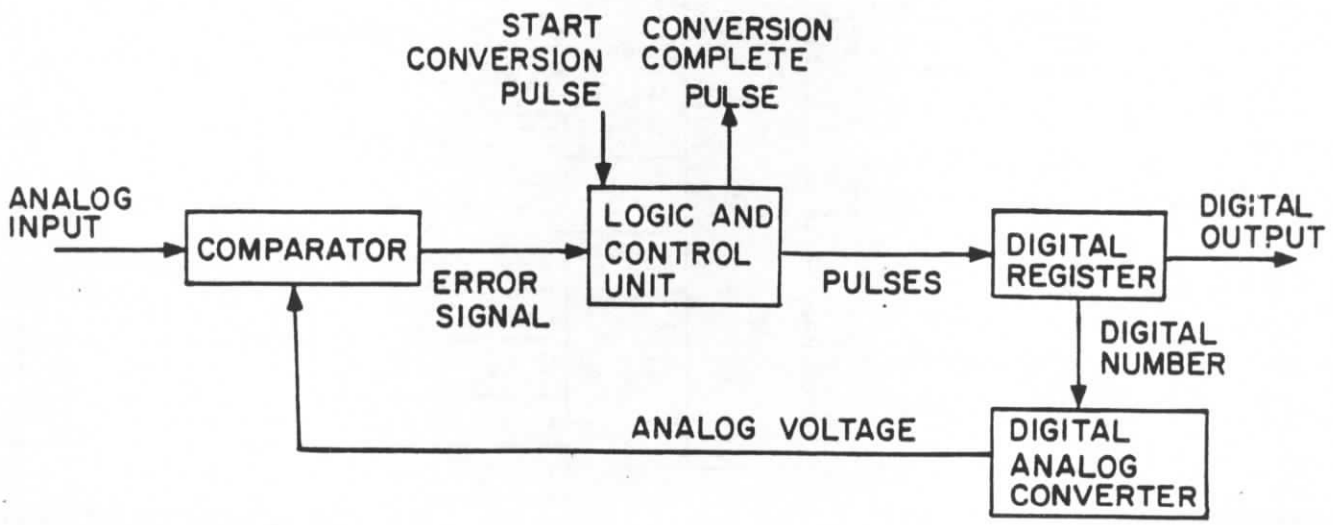

Figure 5.9 Closed-Loop Type Analog/Digital Converter

The comparator output is processed by a simple logic network, usually consisting of a number of gate circuits, such that a sequence of pulses is produced. Each pulse causes the contents of the digital output-register to be modified so as to reduce the error signal. This change in the digital output produces a change in the output of the digital/analog converter, which in turn modifies the output of the comparator circuit. The error signal is thereby reduced progressively until it falls within a specified tolerance. The conversion is then complete, and the logic circuit emits a control pulse. The number within the digital register is then read out, perhaps directly into the digital computer, and a new conversion can begin. The rate at which conversion can be accomplished, i.e., the number of analog samples which can be handled per second, is determined by the manner in which the contents of the digital register are modified in response to an error signal.

There are two major alternatives in the implementation of the closed-loop conversion method. These relate to the manner in which the pulses emitted by the logic circuit are utilized. In the "successive approximation" method, the most-significant bit in the register is modified first; by contrast, in the "incremental method", the least-significant bit in the register is modified first. In the successive-approximation converter, the start pulse, initiating the conversion, causes the contents of the digital register to be reset to zero. The most-significant bit is then changed from "0" to "1". If this change in the contents of the register causes the DAC output to be larger than the analog input, the most-significant bit is reset to zero; if not, the most-significant bit remains at "1". In either case, the second most-significant bit is then changed from "0" to "1" and

the analog voltages and DAC output are again compared. This procedure is repeated for all of the bits in the digital register. The length of time required for a complete conversion is therefore proportional to the word length. Since the digital register is reset to zero before the start of each conversion, the conversion speed is unaffected by the quantity which was stored in the digital register at the completion of the preceeding conversion.

In an incremental converter, the digital register is not reset to zero at the start of a conversion, and the least-significant bit is changed in response to an error signal. Where the analog input voltage undergoes relatively small changes from one conversion to the next, an incremental converter is able to produce an output much more rapidly, since only a very few of the digital-register bits have to be modified. Where large changes in analog input-voltages occur however, as in the case of multiplexed inputs, the incremental converter must laboriously step from one value to another, one least-significant bit at a time. The length of time required for a given conversion is therefore proportional to the change in the analog input from one conversion to the next.

The difference in operation of the successive-approximation and incremental method of analog/digital conversion is illustrated in Figure 5.10 for a six-bit analog/digital converter and a voltage range such that one least-significant bit corresponds to 0.1 volt. While the analog signal is varying slowly, the incremental converter can keep us with the input and provides many more outputs than does the successive-approximation converter. On the other hand, where the analog signal undergoes abrupt changes, the incremental converter must approach the new values in steps of one

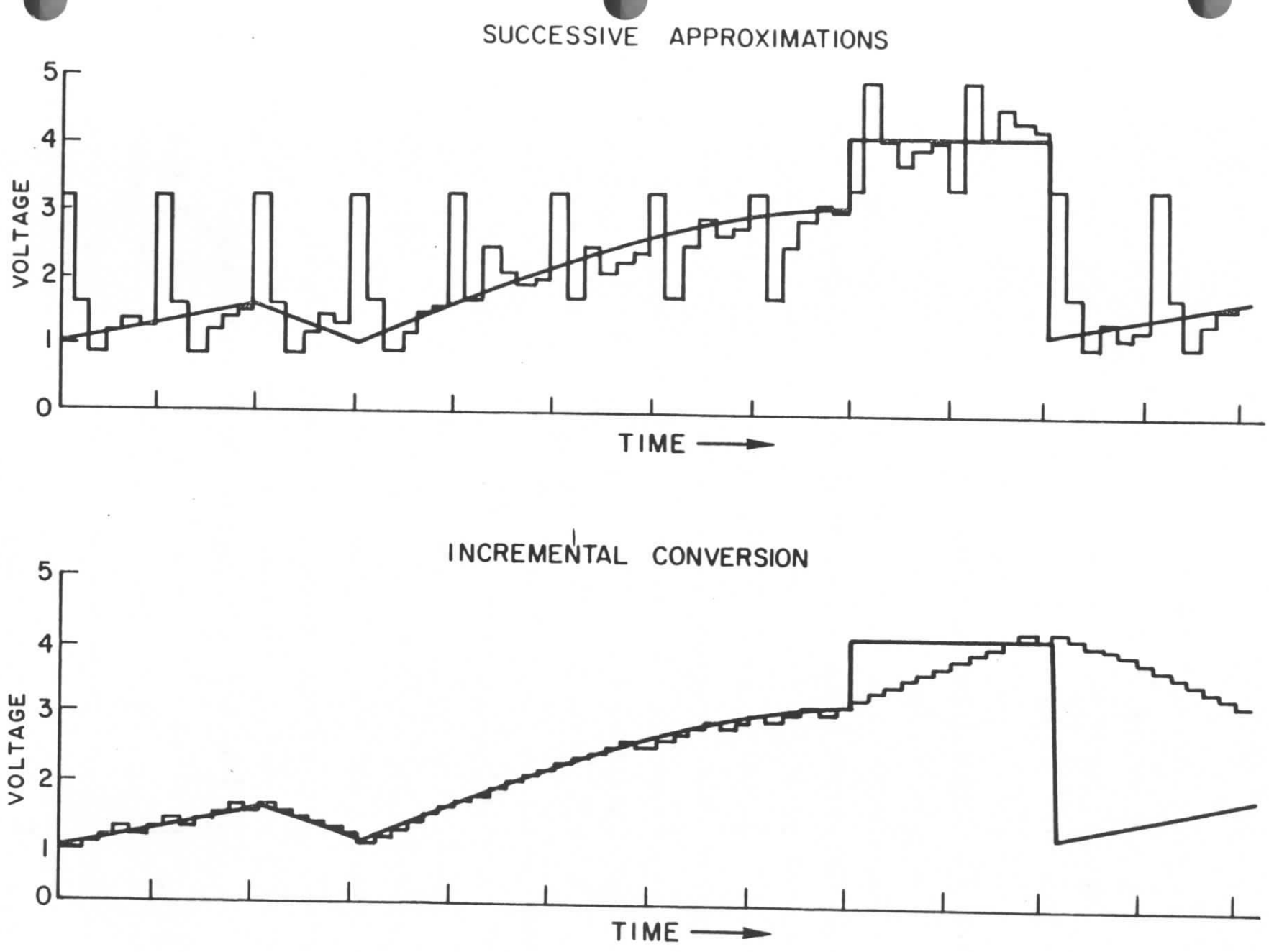

FIGURE 5.10

Input/Output Characteristics of Analog/Digital Converters
Working by Successive Approximations and Incrementally

least-significant bit, at a great expenditure of time. For the successive-approximation converter, abrupt changes in input voltage present no special problem, and a readout is available after every six clock-pulses regardless of the nature of the input.

5.8 Analog/Digital Conversion by Subranging

The closed-loop converters described in the preceding section use only one comparator and are therefore more economical than the simultaneous converter described in Section 5.6. The time for an n-bit conversion however is necessarily at least n cycle times (or the time for n clock pulses). To increase the conversion speed, a new class of analog/digital converters was introduced. These represent a compromise between the closed-loop and the simultaneous-conversion approaches. A simplified block diagram of a subranging analog/digital converter is shown in Figure 5.11.

During the first conversion cycle, digital/analog converter 1 is set to the maximum output value while digital/analog converter 2 is set to zero. The full voltage range, E, therefore appears across the resistance network, and comparators C_1, C_2, C_3,...C_7 receive inputs of 1/8 E, 2/8 E, 3/8 E,... 7/8 E respectively. The other input of each comparator is the analog voltage to be converted. The voltage levels assumed by the seven comparators are processed by the logic network and translated into the digital output. To this point, the system acts exactly like a simultaneous analog/digital converter with a three-bit digital register, and in fact the result of the first conversion cycle determines the three most significant bits of the digital output. In the next conversion step, however, the entire resistance network is employed to subdivide a small portion of the full voltage range.

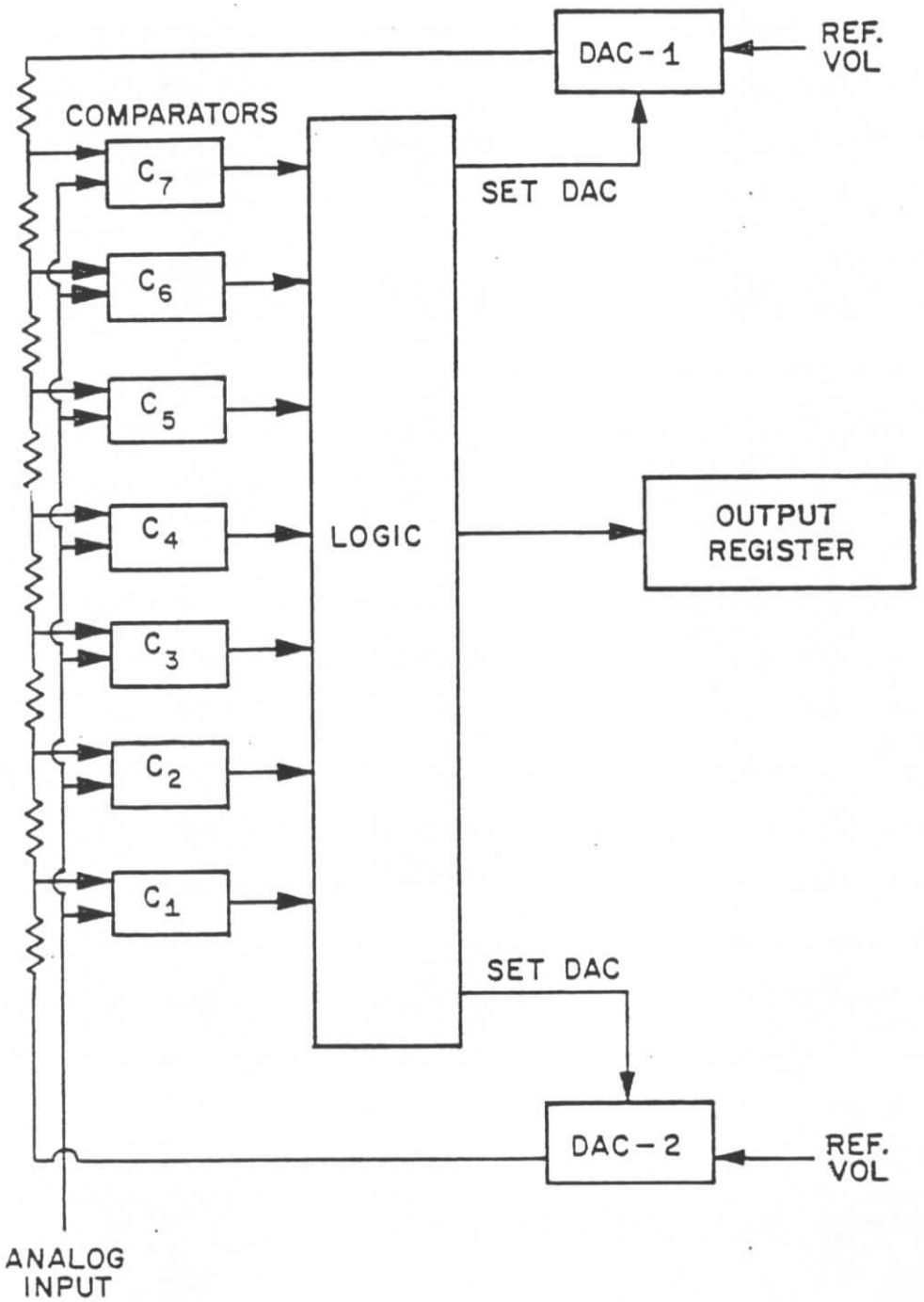

FIGURE 5.11

Sub-ranging Type Aralog/Digital Converter

Consider, for example, that the analog input voltage is 0.525E. In that case, the analog input is greater than the reference input for comparators C_1, C_2, C_3, and C_4, while it is less than the reference input for comparators C_5, C_6 and C_7. The latter three comparators therefore have negative output levels while the first four comparators have positive output levels. At this juncture, the converter has established that the analog input lies betweeen 0.5000 E and 0.6250 E.

In the next step of the conversion cycle, digital/analog converter 1 is set to 0.6250 E, and digital/analog converter 2 is set to 0.5000 E. The reference inputs of the comparators C_1, C_2, C_3,...C_7 now become approximately 0.5156 E, 0.5312 E, 0.5468 E, ..., 0.609E, respectively, so that the voltage range that formerly existed between the reference voltages of C_4 and of C_5 is now divided into eight equal steps. The analog input has remained at 0.525E, so that the second conversion-step determines that the unknown falls between 5.156 E and 0.5312 E, effectively establishing the fourth, fifth, and sixth most-significant bits of the digital output. The two values, 0.5156 E and 0.5312 E, are now applied to digital/analog converter 2 and digital/analog converter 1 respectively to start the third conversion step. In this way, each successive conversion-step determines an additional three digits of the digital output. If seven comparators are used, the subranging converter is approximately three times as rapid as a closed-loop successive-approximation converter.

5.9 Time-Interval Analog/Digital Converter

The last method of analog/digital conversion to be described in this chapter is too slow to be useful for many real-time applications. Time-